IN THE CLAIMS:

1. (canceled)

2. (currently amended) ~~The~~ A near-hermetic power chip-on-board (P-COB) device ~~according to claim 1, wherein said~~ comprising:

a substrate ~~is~~ formed at least in part from a polyimide PWB;

a semiconductor device disposed on said substrate, said semiconductor device including a silicon nitride passivation upper layer; and

a sealant disposed directly on said silicon nitride layer.

3. (currently amended) ~~The~~ A near-hermetic power chip-on-board (P-COB) device ~~according to claim 1, wherein said~~ comprising:

a substrate ~~is~~ formed at least in part from a direct bond copper substrate;

a semiconductor device disposed on said substrate, said semiconductor device including a silicon nitride passivation upper layer; and

a sealant disposed directly on said silicon nitride layer.

4. (currently amended) The P-COB device according to claim [[1]] 2, further comprising:

a die attachment which attaches said semiconductor device to said substrate.

5. (currently amended) ~~The~~ A near-hermetic power chip-on-board (P-COB) device ~~according to claim 1, wherein said~~ comprising:

a substrate;

a semiconductor device disposed on said substrate, said semiconductor device including a silicon nitride passivation upper layer; and

a sealant disposed directly on said silicon nitride layer sealant ~~is~~ formed ~~of~~ at least part from silicon carbide.

6. (original) The P-COB device according to claim 5, wherein said silicon carbide is deposited at a thickness of approximately 4000 Angstroms.

7. (currently amended) ~~The~~ A near-hermetic power chip-on-board (P-COB) device ~~according to claim 1, further~~ comprising:

a substrate;

a semiconductor device disposed on said substrate, said semiconductor device including a silicon nitride passivation upper layer;

a sealant disposed directly on said silicon nitride layer sealant; and

an aluminum bond pad and aluminum wires disposed on said semiconductor device.

8. (original) The P-COB device according to claim 7, further comprising:

a conformal coating disposed on said sealant, said aluminum bond pad and said aluminum wires.

9. (original) The P-COB device according to claim 8, further comprising:

a protective cover disposed on said conformal coating.

10. (currently amended) ~~The~~ A near-hermetic power chip-on-board (P-COB) device ~~according to claim 1, wherein said~~ comprising:

a substrate;

a semiconductor device ~~is~~ comprising a power MOSFET disposed on said substrate, said semiconductor device including a silicon nitride passivation upper layer; and

a sealant disposed directly on said silicon nitride layer sealant.

11. (original) The P-COB device according to claim 8, wherein said conformal coating is less than 2 mils in thickness.

12. (original) A near-hermetic device comprising:

a substrate;

an electronics package disposed on said substrate;

a sealant disposed directly on a surface of said electronics package; and

a conformal coating disposed on said sealant.

13. (original) The near-hermetic device according to claim 12, further comprising:

a protective cover disposed on said conformally-coated electronics package.

14. (original) A power chip-on-board (P-COB) device comprising:

a substrate;

a semiconductor device disposed on said substrate, said semiconductor device including a silicon nitride passivation upper layer;

a silicon carbide layer disposed directly on said silicon nitride layer; and

a conformal coating disposed on said silicon carbide layer.

15. (canceled)

16. (currently amended) ~~The~~ A method of manufacturing a near-hermetic power-chip-on-board (P-COB) device ~~according to claim 14, further~~ comprising:

providing a substrate;

attaching a semiconductor device to said substrate;

directly depositing a sealant over an upper passiviation layer of silicon nitride of said semiconductor device; and

disposing an aluminum bond pad and aluminum wires on said semiconductor device.

17. (original) The method according to claim 16, further comprising:

disposing a conformal coating on said sealant.

18. (original) The method according to claim 17, further comprising:
disposing a protective cover on said conformal coating.

19. (currently amended) The method according to claim [[15]] 16, wherein said semiconductor device is a power MOSFET.

20. (currently amended) The method according to claim [[15]] 16, wherein said substrate is a polyimide PWB.

21. (currently amended) The method according to claim [[15]] 16, wherein said substrate is a direct bond copper substrate.

22. (currently amended) The method according to claim [[15]] 16, further comprising:
attaching said semiconductor device to said substrate using a die attachment.

23. (currently amended) The method according to claim [[15]] 16, wherein said sealant is a silicon carbide.

24. (original) The method according to claim 23, wherein said silicon carbide is deposited to a thickness of approximately 4000 Angstroms.